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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/450,802	11/29/1999	JAY SETHURAM	STRAT-P013	8198

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EXAMINER	
DUONG, DUC T	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/450,802	SETHURAM, JAY	
	Examiner	Art Unit	
	Duc T. Duong	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21 and 22* is/are allowed.

6)☒ Claim(s) *1-3,6,7,9-11 and 14-19* is/are rejected.

7)☒ Claim(s) *4,5,8 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 6, 7, 9, 14, 18, and 19 have been considered but are moot in view of the new ground(s) of rejection. The examiner would also like to point out to applicant in the specification page 5 lines 18-23, applicant has indicated that network protocol layers can be implemented on integrated circuit. Thus, the examiner has taken this admission in considering the new ground of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6, 7, 9-11, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa (US Patent 5,748018) in view of Cannella, Jr. (US Patent 5,668,810).

Regarding to claims 1-3, Ishikawa discloses a source synchronous clocking system (Fig. 3A), comprising a source clock domain in a first integrated circuit 100 (Fig. 3A), comprising a register 101 having a first input D for receiving a data signal (Fig. 3A col. 4 lines 2-3), a second input CK for receiving a clock signal (Fig. 3A col. 4 lines 3-5), and an output Q (Fig. 3A col. 4 lines 5-8); a buffer 103 having an input CLK for receiving the clock signal and an output 105 (Fig. 3A col. 4 lines 10-14), said buffer generating a delay t_{b103} that is substantially equivalent to a delay through said register (Fig. 3B col. 5

lines 10-12; noted from the timing diagram the buffer delay t_{b103} is substantially equivalent to the data transfer (register) delay t_D); and a first transmit and receive clock domain 100 for transmitting the data D and clock signals CK to said a second transmit and receive clock domain 200 (Fig. 3A); and a destination clock domain in a second integrated circuit 200 (Fig. 3A), comprising a register 201 having a first input D and a second input CK, the first input of said register of said destination clock domain being coupled to the output of said register in the source clock domain (Fig. 3A col. 4 lines 47-49),

Ishikawa fails to teach for the first integrated circuit comprising a PHY layer and the second integrated circuit comprising a link layer.

However, Cannella discloses a data communication system equipped with application specific integrated circuit ASIC for implementing a link network protocol layer and a physical network protocol layer (fig. 1 col. 4 lines 43-47).

Thus, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to implement a link layer and a physical layer in an IC circuit as taught by Cannella since such implementation is well known in the art in designing network communication equipments.

Regarding to claims 6 and 18, Ishikawa discloses a serial termination circuit (Fig. 4A; one of terminating resistor 322 and 326 form a serial termination circuit) for absorbing a reflection generated by the data signal (col. 7 lines 10-16).

Regarding to claims 7 and 19, Ishikawa discloses a parallel termination circuit (Fig. 4A; both terminating resistor 322 and 326 form a parallel termination circuit) for absorbing a reflection generated by the data signal (col. 7 lines 10-16).

Regarding to claims 9-11, Ishikawa discloses a method for operating a source synchronous clocking system between a first integrated circuit 100 and a second integrated circuit 200 from a source clock 104 (Fig. 3A), comprising receiving an input clock signal CK in a first clock domain in a first integrated circuit 100 (Fig. 3A col. 4 lines 3-5); receiving an input data signal D in the first clock domain in the first integrated circuit 100 (Fig. 3A col. 4 lines 2-3); latching the input data signal by triggering the input data signal by the input clock signal (Fig. 3B col. 4 lines 55-62); delaying the input clock signal by an amount that is equal to the delay in the latching device (Fig. 3B col. 5 lines 10-12; noted from the timing diagram the buffer delay t_{b103} is substantially equivalent to the data transfer (register) delay t_D); and generating an output clock signal 105 and an output data signal 106 in the second clock domain in the second layer 200 (Fig. 3A col. 4 lines 41-47), the output clock signal and the output data signal being synchronized to each other (Fig. 3b col. 4 lines 55-65).

Ishikawa fails to teach for the first integrated circuit comprising a PHY layer and the second integrated circuit comprising a link layer.

However, Cannella discloses a data communication system equipped with application specific integrated circuit ASIC for implementing a link network protocol layer and a physical network protocol layer (fig. 1 col. 4 lines 43-47).

Thus, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to implement a link layer and a physical layer in an IC circuit as taught by Cannella since such implementation is well known in the art in designing network communication equipments.

Regarding to claims 14-17, Ishikawa discloses a method for providing a clock input and a data input synchronously between a first 100 and second integrated circuit 200 (Fig. 3A), comprising the steps of receiving the clock input CK (Fig. 3A col. 4 lines 3-5); receiving the data input D (Fig. 3A col. 4 lines 2-3); transmitting the clock input to a latching device for triggering the data input (Fig. 3B col. 4 lines 55-62); sending the clock input through a buffer (Fig. 3A col. 4 lines 5-8), the buffer having a delay which is equal to the delay through the latching device (col. 4 lines 10-14); and generating an output data from the latching device that synchronizes with an output clock from the buffer (Fig. 3B col. 4 lines 55-65).

Ishikawa fails to teach for the first integrated circuit comprising a PHY layer and the second integrated circuit comprising a link layer.

However, Cannella discloses a data communication system equipped with application specific integrated circuit ASIC for implementing a link network protocol layer and a physical network protocol layer (fig. 1 col. 4 lines 43-47).

Thus, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to implement a link layer and a physical layer in an IC circuit as taught by Cannella since such implementation is well known in the art in designing network communication equipments.

Allowable Subject Matter

4. Claims 4, 5, 8, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 21 and 22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or make obvious the steps of or means for **"a delay circuit, coupled between said source clock domain and said destination clock domain, for introducing additional delay to the clock signal"**, when such delay circuit is considered within the specific structure of the device recited in claims 4 and 21. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or make obvious the steps of or means for **"a second buffer having an input coupled to an output of said delay circuit and an output coupled to said register in said destination clock domain"**, when such buffer is considered within the specific structure of the device recited in claim 5. The prior art of record fails to teach or make obvious the steps of or means for **"the clock signal generated from the output of the second buffer is connected to a clock input of in said destination clock domain"**, when such clock signal is considered within the specific structure of the device recited in claim 8. The prior art of record fails to teach or make obvious the steps of or means for **"generating control signals of the data input, the control signals being multiplexed with the data input"**, when such

control signals are considered within the specific structure of the device recited in claim 20 and 22.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Duong whose telephone number is 571-272-3122. The examiner can normally be reached on M-F (9:00 AM-5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD
DD

RICKY NGO
PRIMARY EXAMINER
6/21/05